In the Claims

Please cancel claims 1 – 64, 66, 68, 70 – 73, 75-78, and 80 and add the following new claims:

- - 81. The voltage pump of claim 65 wherein each of said plurality of voltage pump circuits includes two substantially identical pump portions operating in tandem, one of said pump portions being responsive to a high condition of said clock signal and the other of said pump portions being responsive to a low condition of said clock signal.

82. The voltage pump of claim 65 wherein said oscillator includes a ring oscillator comprised of inverters connected in a ring for producing said clock signal.

83. The voltage pump of claim 82 wherein said oscillator includes a plurality of multiplexers responsive to various tap points in said ring, and wherein said multiplexers produce a clock signal of variable frequency dependent upon the tap point selected to produce said clock signal.

84. The voltage pump of claim 65 additionally comprising a second regulator circuit for producing second signals for controlling said oscillator circuit, and a regulator select circuit for selecting one of said first and said second signals for input to said oscillator.

85. A voltage pump for a dynamic random access memory, comprising:

a variable pump for supplying power at variable levels in response to a clock signal and an enable signal produced by the dynamic random access memory;

an oscillator for producing said clock signal; and

a regulator for producing first signals for controlling said oscillator means.

86. The voltage pump of claim 85 wherein said variable pump includes a first and second plurality of individual pump circuits, each pump circuit including two substantially identical pump portions operating in tandem in response to said clock signal.

87. The voltage pump of claim 86 wherein said first plurality and said second plurality of voltage pump circuits are operable when the dynamic random access memory is in a first type of refresh mode and wherein only said first plurality of voltage pump circuits is operable when the dynamic random access memory is in a second type of refresh mode.

88. The voltage pump of claim 87 wherein the first type of refresh mode includes a 4k refresh mode and wherein said second type of refresh mode includes an 8k refresh mode.

89. The voltage pump of claim 87 wherein said first plurality of voltage pump circuits includes six voltage pump circuits and wherein said second plurality of voltage pump circuits includes another six voltage pump circuits.

90. The voltage pump of claim 85 wherein said oscillator includes a ring oscillator comprised of inverters connected in a ring for producing said clock signal.

91. The voltage pump of claim 90 wherein said oscillator includes a plurality of multiplexers responsive to various tap points in said ring, and wherein said multiplexers produce a clock signal of variable frequency dependent upon the tap point selected to produce said clock signal.

92. The voltage pump of claim 85 additionally comprising a second regulator for producing second signals for controlling said oscillator, and a regulator select circuit for selecting one of said first and said second signals for input to said oscillator.

93. The voltage pump of claim 85 wherein said voltage pump produces a boosted wordline voltage of variable output power.

94. A method of controlling a voltage pump for a dynamic random access memory, comprising the steps of:

providing a boosted voltage at a first power level in response to a first refresh mode; and

providing said boosted voltage at a second power level in response to a second refresh mode.

95. A method of operating a voltage pump for an integrated circuit, comprising the steps of:

producing a clock signal;

providing power with a first plurality of voltage pump circuits in response to said clock signal;

producing an enable signal whenever a higher level of power is needed; and

selectively providing power with a second plurality of voltage pump circuits in response to said clock signal and said enable signal.

96. The stability sensor of claim 67 wherein said overcurrent circuit includes two series connected inverters responsive to said resistor.

97. In combination, a stability sensor and a voltage generator, said combination comprising:

a voltage generator for generating an output voltage;

a voltage detection circuit responsive to the output voltage for producing a first and a second signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to the first and second signals for providing an indication of the stability of the voltage generator.

98. The combination of claim 97 wherein said voltage generator includes:

an output terminal at which the output voltage is available;

a first feedback circuit responsive to the output voltage for generating a pullup signal whenever the output voltage falls below a predetermined value;

a second feedback circuit responsive to the output voltage for generating a pulldown signal whenever the output voltage rises above another predetermined value;

a first circuit responsive to the pullup signal for increasing the output voltage; and

a second circuit responsive to the pulldown signal for decreasing the output voltage.

99. The combination of claim 98 wherein said first feedback circuit includes a group of series connected pMOS transistors responsive to the output voltage and wherein said second feedback circuit includes a group of series connected nMOS transistors responsive to the output voltage, and wherein said first and second feedback circuits are interconnected by a bias circuit.

100. The combination of claim 99 wherein said pullup signal is filtered before being input to said first circuit.

101. The combination of claim 100 wherein said first circuit includes an n-type transistor for connecting a source of power to said output terminal, said n-type transistor having a gate terminal for receiving said filtered pullup signal.

102. The combination of claim 100 wherein said pulldown signal is filtered before being input to said second circuit.

103. The combination of claim 102 wherein said second circuit includes a p-type transistor for connecting a ground potential to said output terminal, said p-type transistor having a gate terminal for receiving said filtered pulldown signal.

104. In combination, a stability sensor and a voltage generator for generating a bias voltage for use in a dynamic random access memory, said combination comprising:

a voltage generator for generating the bias voltage;

a voltage detection circuit responsive to the bias voltage for producing a first and a second signal indicative of whether the bias voltage is within a first predetermined range; and

a logic circuit responsive to the first and second signals for providing an indication of the stability of the voltage generator.

105. The combination of claim 104 wherein said voltage detection circuit includes:

a first transistor responsive to the bias voltage for producing said first signal indicative of whether the bias voltage is greater than an upper limit of said first predetermined range; and

a second transistor responsive to the bias voltage for producing said second signal indicative of whether the bias voltage is less than a lower limit of said first predetermined range.

106. The combination of claim 104 wherein said voltage generator produces a pullup and a pulldown current for regulation purposes, said combination further comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

107. The combination of claim 106 wherein said pullup current monitor includes:

a source circuit for sourcing current, each source current being indicative of the present pullup current,

a sink circuit for sinking current;

an RC time constant circuit connected between said source circuit and said sink circuit such that each sink current is indicative of a previous pullup current;

a positive differential current circuit responsive to the source current and the sink current for generating said first pullup signal indicative of whether the present pullup current is greater than the previous pullup current; and

a negative differential current circuit responsive to the source current and the sink current for generating said second pullup signal indicative of whether the present pullup current is less than the previous pullup current.

108. The combination of claim 107 wherein said sink circuit includes a transistor controlled by said RC time constant circuit.

109. The combination of claim 107 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the source and the sink current.

110. The combination of claim 107 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and an inverter responsive to said voltage.

111. The combination of claim 107 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and a pair of series connected inverters responsive to said voltage.

112. The combination of claim 106 wherein said pulldown current monitor includes:

a sink circuit for sinking current, each sink current being indicative of the present pulldown current;

a source circuit for sourcing current;

an RC time constant circuit connected between said sink circuit and said source circuit such that each source current is indicative of a previous pulldown current;

a positive differential current circuit responsive to the sink current and the source current for generating said first pulldown signal indicative of whether the present pulldown current is greater than the previous pulldown current; and

a negative differential current circuit responsive to the sink current and the source current for generating said second pulldown signal indicative of whether the present pulldown current is less than the previous pulldown current.

113. The combination of claim 112 wherein said source circuit includes a transistor controlled by said RC time constant circuit.

114. The combination of claim 112 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the sink current and the source current.

115. The combination of claim 112 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and an inverter responsive to said voltage.

116. The combination of claim 112 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and a pair of series connected inverters responsive to said voltage.

117. A method of determining the stability of a voltage generator generating an output voltage and using pullup and pulldown currents for control purposes, comprising the steps of:

producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range;

generating a first pullup signal and a second pullup signal indicative of whether the change over time in the pullup current is within a second predetermined range;

generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range; and

combining said overvoltage signal, said under voltage signal, said first and second pullup signals, and said first and second pulldown signals to provide an indication of the stability of the voltage generator.

118. The method of claim 117 wherein said step of generating a first pullup signal and a second pullup signal includes the steps of:

sourcing currents, each current being indicative of the present pullup current;

sinking currents;

charging a capacitor with the difference between the source currents and the sink currents such that the sink currents are indicative of a previous pullup current;

comparing the present pullup current and the previous pullup current; and

generating said first pullup signal when the present pullup current is greater than the previous pullup current and generating said second pullup signal when the present pullup current is less than the previous pullup current.

119. The method of claim 117 wherein said step of generating a first pulldown signal and a second pulldown signal includes the steps of:

sinking currents, each current being indicative of the present pulldown current;

sourcing currents;

charging a capacitor with the difference between the sink currents and the source currents such that the source currents are indicative of a previous pulldown current;

comparing the present pulldown current and the previous pulldown current; and

generating said first pulldown signal when the present pulldown current is greater than the previous pulldown current and generating said second pulldown signal when the present pulldown current is less than the previous pulldown current.

120. The method of claim 117 additionally comprising the step of generating an overcurrent signal in response to one of an excessive pullup current condition and an excessive pulldown current condition.

121. The powerup circuit of claim 69, wherein said first circuit portion includes:

a first voltage detector constructed of p-type components and responsive to the external voltage for producing a first signal indicative of the external voltage being greater than said predetermined value;

a second voltage detector constructed of n-type components and responsive to the external voltage for producing a second signal indicative of the external voltage being greater than said predetermined value; and

a logic circuit responsive to said first and second signals for producing said first output signal.

122. The powerup circuit of claim 69, wherein said second circuit portion includes:

a logic circuit responsive to said first output signal and the feedback signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

123. The powerup circuit of claim 69, additionally comprising a reset circuit interposed between said first and second circuit portions for receiving said first output signal from said first circuit portion and for terminating said first output signal when predetermined stability requirements are not meet.

124. A powerup circuit in combination with a plurality of voltage supplies receiving an external voltage and an initial feedback signal, said combination comprising:

a first circuit responsive to the external voltage for producing a first output signal indicative of whether the external voltage is within a predetermined range;

a reset circuit for conducting said first output signal when said first output signal is within said predetermined range for a predetermined period of time;

a second circuit responsive to said conducted first output signal and the initial feedback signal for producing a first enable signal;

a first voltage supply for powering up in response to said first enable signal and for producing a first output voltage and a first feedback signal indicative of whether said first voltage supply is in a predetermined operating state;

a third circuit responsive to said conducted first output signal, the initial feedback signal, and said first feedback signal for producing a second enable signal; and

a second voltage supply responsive to said second enable signal for producing a second output voltage.

125. A powerup sequence circuit for controlling the sequence of powering up a bias generator and a voltage pump of a dynamic random access memory having a back bias voltage pump and being supplied with a supply voltage external to the memory, said powerup sequence circuit comprising:

means for generating a status signal indicative of the status of the supply voltage externally supplied;

means for generating a first enable signal in response to the condition of the back bias voltage pump and said status signal, said first enable signal being input to the bias generator; and

means for generating a second enable signal in response to the condition of the back bias voltage pump, said status signal, and the condition of the bias generator, said second enable signal being input to the voltage pump.

126. The powerup sequence circuit of claim 125 wherein said memory includes a row address strobe (RAS) buffer, and wherein said powerup sequence circuit additionally comprises means for generating a third enable signal in response to the condition of the back bias voltage pump, said status signal, the condition of the bias generator, and the condition of the voltage pump, said third enable signal being input to the RAS buffer.

127. The powerup sequence circuit of claim 126 additionally comprising means for generating a powered-up signal in response to the condition of the back bias voltage pump, said status signal, the condition of the bias generator, the condition of the voltage pump, and said third enable signal, said powered-up signal being used by said memory device.

128. The powerup sequence circuit of claim 125 additionally comprising means for generating an alternate first enable signal and an alternate second enable signal based on a time

constant, and means for selecting between said first and said second enable signals and said alternate first and second enable signals.

129. The powerup sequence circuit of claim 125 additionally comprising means for determining the stability of said status signal.

130. A method for controlling the powering up of a first voltage supply in response to first and second external signals, comprising the steps of:

generating a first output signal indicative of whether the first external signal satisfies a first predetermined condition;

generating an enable signal in response to said first output signal and the second external signal; and

inputting said enable signal to the first voltage supply to enable the first voltage supply to become operative.

131. The method of claim 130 wherein said step of generating a first output signal includes the step of generating said first output signal when the external voltage is greater than a predetermined voltage.

132. The method of claim 131 additionally comprising the step of terminating said first output signal when said first output signal fails to satisfy predetermined stability requirements.

133. The method of claim 130 for controlling the power up of a second voltage supply in response to a third external signal, further comprising the steps of:

generating a second enable signal in response to said first output signal, the second external signal, and the third external signal; and

inputting said second enable signal to the second voltage supply to enable the second voltage supply to become operative.

134. A method of controlling the powering up of two voltage supplies of an integrated circuit in response to an externally applied voltage to the integrated circuit and an initial feedback signal, comprising the steps of:

generating a first output signal when the applied voltage satisfies a predetermined condition;

enabling a first voltage supply to power up and to generate a first feedback signal based on the condition of the first voltage supply in response to said first output signal and said initial feedback signal; and

enabling the second voltage supply to power up in response to said first output signal, the initial feedback signal, and said first feedback signal.

135. The method of claim 134 for controlling the powering up of a third voltage supply, additionally comprising the steps of:

generating a second feedback signal based on the condition of the second voltage supply; and

enabling the third voltage supply in response to said first output signal, the initial feedback signal, said first feedback signal, and said second feedback signal.

136. The method of claim 135 additionally comprising the steps of:

generating a third feedback signal based on the condition of the third voltage supply; and

enabling a buffer in response to said first output signal, the initial feedback signal, and said first, second, and third feedback signals.

137. The method of claim 136 additionally comprising the step of signaling the completion of the powerup sequence in response to said buffer enable signal, said first output signal, the initial feedback signal, and said first, second, and third feedback signals.

138. A method for controlling the sequence of powering up a dynamic random access memory having a back bias voltage pump, a cell plate bias generator, and a voltage pump, the dynamic random access memory being supplied with an external supply voltage, said method comprising the steps of:

generating a status signal indicative of the status of the supply voltage;

generating a first enable signal in response to the condition of the back bias voltage pump and said status signal;

inputting said first enable signal to the cell plate bias generator to power up the cell plate bias generator;

generating a second enable signal in response to the condition of the back bias voltage pump, said status signal, and the condition of the cell plate bias generator; and

inputting said second enable signal to the voltage pump to power up the voltage pump.

139. The method of claim 138 wherein the memory device includes a row address strobe (RAS) buffer, said method additionally comprising the steps of:

generating a third enable signal in response to the condition of the back bias voltage pump, said status signal, the condition of the cell plate bias generator, and the condition of the voltage pump; and

inputting said third enable signal to the RAS buffer to power up the RAS buffer.

140. The method of claim 139 additionally comprising the step of generating a powered-up signal in response to the condition of the back bias voltage pump, said status signal, the condition of the cell plate bias generator, the condition of the voltage pump, and said third enable signal.

141. The method of claim 138 additionally comprising the steps of:

generating an alternate first enable signal and an alternate second enable signal based on a time constant; and

selecting between said first and second enable signals and said alternate first and second enable signals.

142. In an electronic circuit having a boot capacitor being driven between high and low states, and having a holding transistor for supplying charge to the boot capacitor, the improvement comprising:

a circuit path connected between the holding transistor and the boot capacitor to ensure the holding transistor is turned off before the boot capacitor is driven to a low state.

143. The improvement of claim 142 wherein said circuit path is self-timed by being responsive to the state of the holding transistor.

144. The improvement of claim 142 wherein said self-timed circuit path includes a logic gate having an output terminal coupled with the capacitor and having input terminals connected so that a signal available at said output terminal maintains a high value when the holding transistor is on.

145. The improvement of claim 144 wherein the electronic circuit in which the improvement is made is an output buffer circuit, and wherein the holding transistor is a field effect transistor having its source to drain path connected with a first side of the capacitor, said self-timed circuit path being coupled between a gate of the holding transistor and a second side of the capacitor.

146. The improvement of claim 145 wherein said logic gate includes a NAND gate having input logic signals representing, at a first input terminal thereof, one of an on and off condition of the holding transistor and, at a second input terminal thereof, one of a high or low level, an output terminal of said NAND gate being coupled to the second side of the capacitor.

147. The improvement of claim 146 wherein said circuit path includes an inverter having an input terminal connected with the gate of the holding transistor, and wherein said first input terminal of said NAND gate receives a signal from said inverter whereby a high signal is input to said NAND gate when the holding transistor is off.

148. A circuit, comprising:

a boot capacitor;

a holding transistor for supplying charge to the boot capacitor;

a circuit for discharging said boot capacitor; and

a self timed circuit path connected between said holding transistor and said boot capacitor.

149. The circuit of claim 148 wherein said circuit path includes a logic gate having an output terminal coupled with said capacitor and having input terminals connected so that a signal available at said output terminal maintains said capacitor charged when said holding transistor is conductive.

150. The circuit of claim 149 wherein said holding transistor is a field effect transistor having its source to drain path connected with a first side of said capacitor, said circuit path being coupled between a gate of said holding transistor and a second side of the capacitor.

151. The circuit of claim 150 wherein said logic gate includes a NAND gate having input logic signals representing, at a first input terminal thereof, one of an on and off condition of the holding transistor and, at a second input terminal thereof, one of a high and low level, an output terminal of said NAND gate being coupled to the second side of the capacitor.

152. The circuit of claim 151 wherein said circuit path includes an inverter having an input terminal connected with said gate of said holding transistor, and wherein said first input terminal of said NAND gate receives a signal from said inverter whereby a high signal is input to said NAND gate when said holding transistor is nonconductive.

153. The output buffer of claim 74 wherein said self-timed circuit path includes a logic gate having an output terminal coupled with said capacitor and having a first input terminal

responsive to said holding transistor and a second input terminal responsive to said logic circuit so that a signal available at said output terminal maintains said boot capacitor charged when said holding transistor is on.

154. The output buffer of claim 153 wherein one of said series connected transistors includes a pMOS transistor and wherein said logic circuit includes an inverter for controlling the state of said pMOS transistor in response to the data in said latch, and wherein said second input terminal of said NAND gate is responsive to said inverter.

155. The output buffer of claim 154 wherein said holding transistor includes an nMOS transistor having its source to drain path connected with a first side of said capacitor, said self-timed circuit path being coupled between a gate of said holding transistor and a second side of said capacitor.

156. The output buffer of claim 155 wherein the voltage stored in said boot capacitor is supplied to said pMOS transistor when the pMOS transistor is rendered conductive.

157. The output buffer of claim 156 wherein said voltage supplied by said boot capacitor is approximately one Vth higher than the first voltage supply.

158. An output stage of a memory device, said output stage comprising:

a plurality of output drive transistors connected in series between a first voltage supply and ground;

an output terminal responsive to said series connected transistors;

a latch circuit for receiving data to be output to said output terminal;

a control circuit for generating control signals for controlling the operation of said latch

a logic circuit responsive to said latch circuit for controlling said output drive transistors to drive a voltage at said output terminal to one of a high and low potential representing a logic state of the data to be output;

a capacitor for supplying additional voltage to certain of said drive transistors;

a charging circuit, responsive to said logic circuit for charging said capacitor to a second supply voltage; and

a circuit path connected between said capacitor and said charging circuit.

159. The output stage of claim 158 wherein said circuit path includes a logic gate having an output terminal coupled with said capacitor and having a first input terminal responsive to said charging circuit through an inverter, and a second input terminal responsive to

said logic circuit so that a signal available at said output terminal maintains said capacitor charged while said charging circuit is in an on state.

160. The output stage of claim 159 wherein one of said series connected transistors includes a pMOS transistor and wherein said logic circuit includes a second inverter for controlling the state of said pMOS transistor in response to the data in said latch circuit, and wherein said second input terminal of said NAND gate is responsive to said second inverter.

161. The output stage of claim 160 wherein said charging circuit includes an nMOS transistor having its source to drain path connected with a first side of said capacitor, said circuit path being coupled between a gate of said nMOS transistor and a second side of said capacitor.

162. The output stage of claim 161 wherein said charging circuit includes a second nMOS transistor having its source to drain path connected between another voltage source and said first side of said capacitor for precharging said capacitor.

163. The output stage of claim 161 wherein the voltage stored on said capacitor is supplied to said pMOS transistor when the pMOS transistor is rendered conductive.

164. The output stage of claim 163 wherein said voltage supplied by said capacitor is approximately one Vth higher than the first voltage supply.

165. The output stage of claim 158, additionally comprising:

an output pad; and

an output driver responsive to said output terminal for driving a voltage available on said output pad to be representative of the voltage available at said output terminal.

166. A method of controlling the charge on a boot capacitor within an output buffer of a memory device, said method comprising the steps of:

charging the boot capacitor to a predetermined voltage from a voltage source;

holding the boot capacitor at the predetermined voltage;

supplying the charge on the boot capacitor to a pullup transistor when the pullup transistor is conductive;

disconnecting the boot capacitor from the voltage source when the pullup transistor is conductive;

monitoring said disconnecting step; and

unbooting the boot capacitor after the boot capacitor is disconnected from the voltage source.

167. The method of claim 166 wherein said monitoring step includes the step of sensing the state of a holding transistor used to connect the boot capacitor to the predetermined voltage.

168. A sense amplifier, comprising:

a digitline for connecting an array to I/O lines;

an equalization switch adjacent the array for equilibrating said digitline;

an n-sense amplifier connected across said digitline;

a p-sense amplifier connected across said digitline;

an isolation switch connected between said n-sense and said p-sense amplifier and said equalization switch for isolating said n-sense and p-sense amplifier from the array; and

a connection switch for connecting said digitline to the I/O line.

169. The sense amplifier of claim 168 wherein said isolation switch includes a plurality of transistors, and wherein said transistors are rendered conductive with a control signal that is a boosted version of the voltage used by the array.

170. The sense amplifier of claim 168 wherein said equilibration switch includes a plurality of transistors, and wherein said transistors are rendered conductive with an equalization control signal.

171. A combination, comprising:

an array having a plurality of digitlines extending therethrough; and

a plurality of sense amplifiers connected across said plurality of digitlines, each of said sense amplifiers comprising:

an equalization switch adjacent said array for equilibrating said digitline;

an n-sense amplifier connected across said digitline;

a p-sense amplifier connected across said digitline;

an isolation switch connected between said n-sense and said p-sense amplifier and said equalization switch for isolating said n-sense and p-sense amplifier from said array; and

a connection switch for connecting said digitline to an I/O line.

172. The combination of claim 171 wherein said isolation switch includes a plurality of transistors, and wherein said transistors are rendered conductive with a control signal that is a boosted version of the voltage used by the array.